THE INVENTION CLAIMED IS:

1. A method of testing an integrated circuit comprising:
providing a semiconductor substrate having a semiconductor device provided thereon;
forming a first dielectric layer over the semiconductor substrate;
forming a first channel in the first dielectric layer in contact with the semiconductor device;
forming a first contact pad mask layer;
forming a first contact pad in the first contact pad mask layer in contact with the first channel;
using the first contact pad to test the first channel and the semiconductor device; and
removing the first contact pad mask layer and the first contact pad.

2. The method as claimed in claim 1 additionally comprising:
using a tester having a microprobe; and
wherein:
using the first contact pad includes forming the first contact pad for contact by the microprobe.

3. The method as claimed in claim 1 additionally comprising:
forming the first contact pad mask layer uses a photoresist.

4. The method as claimed in claim 1 additionally comprising:
forming the first contact pad forms a material selected from a group consisting of copper, aluminum, gold, silver, a compound thereof, and a combination thereof.

5. The method as claimed in claim 1 wherein:
removing the first contact pad mask layer and the first contact pad uses polishing.

6. The method as claimed in claim 1 additionally comprising:
forming a second dielectric layer over the semiconductor substrate;
forming a second channel in the second dielectric layer in contact with the semiconductor device;
forming a second contact pad mask layer;
forming a second contact pad in the second contact pad mask layer in contact with the channel;

using the second contact pad to test the second channel; and

removing the second contact pad mask layer and the second contact pad.

7. The method as claimed in claim 6 additionally comprising:

using a tester having a microprobe; and

wherein:

using the second contact pad includes forming the second contact pad for contact by the microprobe.

8. The method as claimed in claim 6 additionally comprising:

forming the second contact pad mask layer uses a photoresist.

9. The method as claimed in claim 6 additionally comprising:

forming the second contact pad uses a material selected from a group consisting of copper, aluminum, gold, silver, a compound thereof, and a combination thereof.

10. The method as claimed in claim 6 wherein:

removing the second contact pad mask layer and the second contact pad uses polishing.

11. The method as claimed in claim 1 additionally comprising:

forming a via dielectric layer over the semiconductor substrate;

forming a via in the via dielectric layer in contact with the semiconductor device;

forming a second dielectric layer over the via dielectric layer;

forming a second channel in the second dielectric layer contiguous with the via;

forming a second contact pad mask layer;

forming a second contact pad in the second contact pad mask layer in contact with the second channel;

using the second contact pad to test the via and second channel; and

removing the second contact pad mask layer and the second contact pad.

12. The method as claimed in claim 11 additionally comprising:

using a tester having a microprobe; and

wherein:

using the second contact pad includes forming the second contact pad for contact by the microprobe.

13. The method as claimed in claim 11 additionally comprising:

forming the second contact pad mask layer uses a photoresist.

14. The method as claimed in claim 11 additionally comprising:

forming the second contact pad forms a material selected from a group consisting of copper, aluminum, gold, silver, a compound thereof, and a combination thereof.

15. The method as claimed in claim 11 wherein:

removing the second contact pad mask layer and the second contact pad uses polishing.

16. A method of testing an integrated circuit comprising:

providing a semiconductor substrate having a semiconductor device provided thereon;

forming a device dielectric layer over the semiconductor substrate by deposition;

forming a first dielectric layer over the device dielectric layer by deposition;

forming a contact to the semiconductor device in the device dielectric layer;

forming a first channel in the first dielectric layer in contact with the contact;

forming a via dielectric layer over the first dielectric layer;

forming a via in the via dielectric layer in contact with the first channel;

forming a second dielectric layer over the via dielectric layer;

forming a second channel in the second dielectric layer contiguous with the via;

forming a contact pad mask layer over a layer selected from the group consisting of the first dielectric layer, the via layer, the second dielectric layer, and a combination thereof;

forming a contact pad in the contact pad mask layer in contact with an element selected from a group consisting of the first channel, the via, the second channel, and a combination thereof;

using the contact pad to test an element from a group consisting of the semiconductor device, the contact, the first channel, the via, the second channel, and a combination thereof; and

removing the contact pad mask layer and the contact pad; and

completing the integrated circuit.

17. The method as claimed in claim 16 additionally comprising:

using a tester having a microprobe; and

wherein:

forming the contact pad includes forming the contact pad for contact by the microprobe.

18. The method as claimed in claim 16 additionally comprising:

forming the contact pad mask layer uses a photoresist.

19. The method as claimed in claim 16 wherein:

forming the contact pad forms a material selected from a group consisting of copper, aluminum, gold, silver, a compound thereof, and a combination thereof.

20. The method as claimed in claim 16 wherein:

removing the contact pad mask layer and the contact pad uses chemical mechanical polishing.